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**Fax Transmittal**

**DATE:** Tuesday, September 14, 2004 1:45:18 PM Total Pages Including Cover: 06

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**TO:** Ofc of Initial Pat Exam Filing Receipt Corrections

**Company:** USPTO

**Fax #:** 1-703-746-9195

**Phone #:**

**Client/Matter #:** 24061. 231

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**FROM:** Bonnie E. Boyle

**Haynes and Boone, LLP**

**Direct Phone #:** 972-739-8660

2505 N. Plano Road

Suite 4000

Richardson, TX 75082-4101

**Direct Fax #:** 972-692-9034

**Main Phone #:** (972) 680-7550

**Main Fax #:** (972) 680-7551

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Syun-Ming Jang, et al.	§	Docket No.:	24061.231
		§		(TSMC2003-1383)
Serial No.:	10/826,899	§		
		§	Examiner:	To Be Determined
Filing Date:	April 16, 2004	§		
		§	Art Unit:	2812
For:	Logic Embedded-Memory	§		
	Integrated Circuits	§	Conf. No.:	2231

VIA FACSIMILE - 1-703-746-9195

Commissioner of Patents

Attention: Office of Initial Patent Examination's Filing Receipt Corrections

PO Box 1450

Alexandria, VA 22313-1450

**REQUEST FOR CORRECTED FILING RECEIPT AND**  
**TRANSMITTAL OF APPLICATION DATA SHEET**

Dear Sir:

Attached is a copy of the official filing receipt received from the United States Patent and Trademark Office in the above-identified patent application in which issuance of a corrected filing receipt is respectfully requested.

A corrected Application Data Sheet is therefore enclosed herewith. Applicants requests correction of the priority data as follows:

This appln claims benefit of 60/548,443 02/27/2004

Applicants respectfully request approval. The Commissioner is hereby authorized to charge any fees or credit any overpayments associated with this communication to Deposit Account No. 13-0824.

Respectfully submitted,



David M. O'Dell

Registration No. 42,044

Date: 9-13-04

HAYNES AND BOONE, LLP  
901 Main Street, Suite 3100  
Dallas, Texas 75202-3789  
Telephone: 972/739-8635  
Facsimile: 214/200-0853

<b>Certificate of Facsimile</b>	
I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office at 703-746-9195 on the date shown below.	
<u>Bonnie Boyle</u>	
Name	
<u>9-14-04</u>	
Date	

## **Application Data Sheet**

### **Application Information**

Application Type::	Regular
Subject Matter::	Utility
Title::	LOGIC EMBEDDED-MEMORY INTEGRATED CIRCUITS
Attorney Docket Number::	24061.231 (TSMC2003-1383)
Request for Early Publication?::	No
Request for Non-Publication?::	No
Suggested Drawing Figure::	2
Total Drawing Sheets::	2
Small Entity::	No
Petition Included?::	No

### **Applicant Information**

Applicant Authority Type::	Inventor
Primary Citizenship Country::	Taiwan, R.O.C.
Status::	Full Capacity
Given Name::	Syun-Ming
Family Name::	Jang
City of Residence::	Hsin-Chu
Country of Residence::	Taiwan, R.O.C.
Street of Mailing Address::	7F, No. 83, Kwung-Hua N. Street Kwung-Hua Li
City of Mailing Address::	Hsin-Chu
Country of Mailing Address::	Taiwan, R.O.C.
Postal or Zip Code of Mailing Address::	300

**Applicant Authority Type::** Inventor  
**Primary Citizenship Country::** Taiwan, R.O.C.  
**Status::** Full Capacity  
**Given Name::** Homg-Huei  
**Family Name::** Tseng  
**City of Residence::** Hsin-Chu  
**Country of Residence::** Taiwan, R.O.C.  
**Street of Mailing Address::** 2F, No. 18-1, Lane 281, Zhong-Yung Rd.  
**City of Mailing Address::** Hsin-Chu  
**Country of Mailing Address::** Taiwan, R.O.C.  
**Postal or Zip Code of Mailing Address::** 300

### Correspondence Information

**Correspondence Customer Number::** 27683  
**Phone Number::** 972.739.8635  
**Fax Number::** 214.200.0853  
**E-Mail Address::** ipdocketing@haynesboone.com

### Representative Information

<b>Representative Customer Number::</b>	27683
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### Domestic Priority Information

<b>Application::</b>	<b>Continuity Type::</b>	<b>Parent Application::</b>	<b>Parent Filing Date::</b>
This Application	claims benefit of	60/548,443	02/27/2004

### Assignee Information

**Assignee Name::** Taiwan Semiconductor Manufacturing Co., Ltd.  
**Street of Mailing Address::** No. 8, Li-Hsin Rd. 6, Science-Based Industrial Park  
**City of Mailing Address::** Hsin-Chu  
**Country of Mailing Address::** Taiwan, R.O.C.  
**Postal or Zip Code of Mailing Address::** 300-77



## UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
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P.O. Box 1450  
Alexandria, Virginia 22313-4450  
www.uspto.gov

APPL NO.	FILING OR 371 (a) DATE	ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/828,899	04/16/2004	2812	1130	24061.231 (TSMC2003-1385)	3	40	3

27683  
HAYNES AND BOONE, LLP  
901 MAIN STREET, SUITE 3100  
DALLAS, TX 75202

CONFIRMATION NO. 2231

## FILING RECEIPT



\*OC000000013084444\*

Date Mailed: 08/28/2004

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-8195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

## Applicant(s)

Syun-Ming Jang, Hsin-Chu, TAIWAN;  
Hong-Huei Tseng, Hsin-Chu, TAIWAN;

## Assignment For Published Patent Application

Taiwan Semiconductor Manufacturing Co., Ltd., Hsin-Chu, TAIWAN;

## Domestic Priority data as claimed by applicant

This appln claims benefit of 60/547,443 02/26/2004 \*  
(\*Data provided by applicant is not consistent with PTO records.

## Foreign Applications

If Required, Foreign Filing License Granted: 06/26/2004

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

## Title

Logic embedded-memory integrated circuits

RECEIVED

JUN 30 2004

HAYNES &amp; BOONE LLP.

Docketed 6.30.04

By cef  
Dmblcs

24061.231  
8.28.04 - 2 mo. resp. to mp due  
1.22.05 - DD resp. to mp due

Preliminary Class  
438

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Title 37, Code of Federal Regulations, 5.11 & 5.15**

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